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2-LAYER, THREE-DIMENSIONAL BARE IC CHIP STRUCTURE

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[There are no amendments to this patent.]

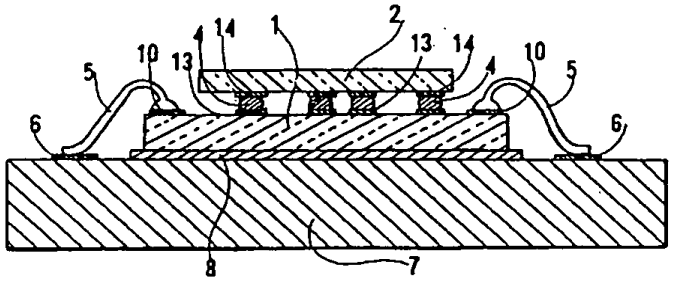
Abstract

Purpose

To provide a chip-mounting structure for the package, substrate, and lead frame that can speed up the circuit operation, increase the mounting density, and dissipate the radiant heat.

Constitution

Symmetrically positioned electrode pads are attached to two chips placed opposite each other and bound together by means of bumps, where one chip is die-bonded to the substrate, etc. The electrode pad of this chip is connected to the substrate pad by wire bonding.



Claim

1. A 2-layer, three-dimensional bare chip structure, characterized in that, on the surface of two semiconductor bare chips, chip electrode pads are formed arranged such that they are turned over and aligned with each other, the respective chip electrodes are connected by means of a conductive bump, the reverse side of one bare chip is die-bonded to a support body of a substrate, lead frame, package, etc., and the electrode pad of the chip which is attached to the reverse side is connected to the substrate pad by means of wire bonding.

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